EMV®
Integrated Circuit Card Specifications for Payment Systems

EMVCo Terminal Type Approval:
Level 1 Mechanical and Electrical Test Cases

Version 4.3a
November 2015

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1 Scope

EMVCo, LLC (‘EMVCo’) is the owner of the EMV Integrated Circuit Card Specification for Payment Systems (version 4.3), hereinafter called EMV Specification.

This specification is divided in 4 books:
- Book 1: Application Independent ICC to Terminal Interface Requirements
- Book 2: Security and Key Management
- Book 3: Application Specification
- Book 4: Cardholder, Attendant, and Acquirer Interface Requirements

The Book 1 (Part II) and Book 2 define the complete flow of a transaction between an Integrated Circuit Card (ICC) and a terminal, from the selection of an application in the ICC to the completion of the transaction.

The Book 3 defines the format of ICC commands used during the transaction flow between the ICC and terminal. Also defined is the transaction flow and associated data for an application compliant with the EMV specifications.

Finally, the Book 4 defines the characteristics of a Terminal that supports an ICC conforming to the two previous specifications mentioned.

EMVCo’s objective is that terminals used for any transaction within the payment systems of EMVCo’s members (i.e. American Express, China UnionPay, Discover Financial Services, JCB, MasterCard International and VISA International) are conform to the EMV Specification.

Within Book 1, Part I of the Integrated Circuit Card Specification for Payment Systems defines electromechanical characteristics, logical interface, and transmission protocols as they apply to the exchange of information between an Integrated Circuit Card (ICC) and a terminal. The purpose of the specification mentioned above is to maximize confidence that ICCs and terminals do not damage each other, and that ICCs and terminals function together correctly up to the point of exchanging information.

The present document, ‘EMVCo Terminal Type Approval: Level 1 Mechanical and Electrical Test Cases’, describes the test cases that, when applied to the IFM part of terminals, are designed to determine whether the IFM meets the mechanical and electrical requirements listed in the Book 1, Part I.

The test cases described cover only the IFM interface as defined in the ‘EMVCo Type Approval – Terminal Level 1 – Administrative Process’ (See [D05]), and test mechanical, electrical and answer to reset requirements. Testing of character transmission, T=0 protocol, and T=1 protocol requirements is described in a separate document. The test cases presented below do not cover the terminal/host interface (if present), general terminal functionality, or other regulatory requirements such as electrical safety or electromagnetic compatibility.

The environment and conditions to be maintained during testing are defined in section 4.3 below. If any special conditions are required for a specific test case, these conditions are described in the test case itself.

The intended audience for this document is testers (EMVCo accredited test laboratories), terminal equipment vendors and qualified auditors.
A testing laboratory that wants to implement and run test cases described in the present document shall follow the rules defined in EMVCo 'Terminal Level 1 Type Approval – Administrative Process' document (See [D05]).
2 Reference Documents

The following are the standards and card approval documentation referenced within the Level 1 Terminal Type Approval process.

2.1 EMVCo Documents

EMV documents are available on the EMVCo website: http://www.emvco.com

The following publications relate to this manual:


[D05] “EMVCo Terminal Type Approval ─ IFM Level 1 Administrative Process”, version 4.3a, November 2015.

[D06] “EMVCo Type Approval ─ Contact Terminal Level 1 ─ Protocol Test Cases”, version 4.3a, November 2015.

[D07] “EMVCo Terminal Type Approval ─ Level 1 Loopback Upper Tester Specification”, version 4.3a, November 2015.

2.2 ISO Standards

The following ISO Standards apply to this document:

<table>
<thead>
<tr>
<th>ISO/IEC 7816 (15 parts)</th>
<th>Identification cards – Integrated circuit cards</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO 5725 (5 parts)</td>
<td>Accuracy (trueness and precision) of measurements methods and results.</td>
</tr>
</tbody>
</table>
3 Glossary of Terms

3.1 Abbreviations and Notations

The following abbreviations and notations are used in this document:

- εΩ: Resistance Measurement Uncertainty of the Test Tool equipment
- ε/%: Duty Cycle Measurement Uncertainty of the Test Tool equipment
- εA: Current Measurement Uncertainty of the Test Tool equipment
- εHz: Frequency Measurement Uncertainty of the Test Tool equipment
- εN: Force Measurement Uncertainty of the Test Tool equipment
- εs: Time Measurement Uncertainty of the Test Tool equipment
- εV: Absolute Voltage Measurement Uncertainty of the Test Tool equipment
- εVV: Voltage Measurement Uncertainty of the Test Tool Equipment for Voltages that are a Function of VCC
- µA: Microampere or 10^-6 A
- µs: Microsecond or 10^-6 s
- Ω: Ohm
- AC: Alternating Current
- ADC: Analogue-Digital Conversion
- APDU: Application Protocol Data Unit
- ATR: Answer To Reset
- BGT: Block Guard Time
- BWI: Block Waiting Time Integer
- BWT: Block Waiting Time
- C-APDU: Command APDU
- CIN: Input Capacitance
- CLA: Class Byte of the Command Message
- CLK: Clock
- C-TPDU: Command TPDU
- CWI: Character Waiting Time Integer
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>CWT</td>
<td>Character Waiting Time</td>
</tr>
<tr>
<td>DAD</td>
<td>Destination Node Address</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>EDC</td>
<td>Error Detection Code</td>
</tr>
<tr>
<td>Etu</td>
<td>Elementary Time Unit</td>
</tr>
<tr>
<td>f</td>
<td>Frequency</td>
</tr>
<tr>
<td>f_i</td>
<td>Average Frequency for the i\textsuperscript{th} Monitoring Interval</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>ICC</td>
<td>Integrated Circuit card</td>
</tr>
<tr>
<td>ICC</td>
<td>Current on the VCC contact</td>
</tr>
<tr>
<td>ICLK</td>
<td>Current on the CLK contact</td>
</tr>
<tr>
<td>ICS</td>
<td>Implementation Conformance Statement</td>
</tr>
<tr>
<td>IO</td>
<td>Current on the I/O contact</td>
</tr>
<tr>
<td>IRST</td>
<td>Current on the RST contact</td>
</tr>
<tr>
<td>ID-1</td>
<td>Identification Card Format</td>
</tr>
<tr>
<td>IFD</td>
<td>Interface Device</td>
</tr>
<tr>
<td>IFM</td>
<td>Interface Module</td>
</tr>
<tr>
<td>IFS</td>
<td>Information Field Size</td>
</tr>
<tr>
<td>IFSC</td>
<td>Information Field Size for the ICC</td>
</tr>
<tr>
<td>IFSD</td>
<td>Information Field Size for the Terminal</td>
</tr>
<tr>
<td>IFSI</td>
<td>Information Field Size Integer</td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current</td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current</td>
</tr>
<tr>
<td>INF</td>
<td>Information Field</td>
</tr>
<tr>
<td>INS</td>
<td>Instruction Byte of Command Message</td>
</tr>
<tr>
<td>IUT</td>
<td>Implementation Under Test</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Output Current</td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Output Current</td>
</tr>
<tr>
<td>ISO</td>
<td>International Organization for Standardization</td>
</tr>
</tbody>
</table>
Glossary of Terms
Abbreviations and Notations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lc</td>
<td>Exact Length of Data Sent by the TAL in a Case 3 or 4 Command</td>
</tr>
<tr>
<td>Le</td>
<td>Maximum Length of Data Expected by the TAL in Response to a Case 2 or 4 Command</td>
</tr>
<tr>
<td>Licc</td>
<td>Exact Length of Data Available in the ICC to be Returned in Response to the Case 2 or 4 Command Received by the ICC</td>
</tr>
<tr>
<td>LEN</td>
<td>Length</td>
</tr>
<tr>
<td>Lr</td>
<td>Length of Response Data Field</td>
</tr>
<tr>
<td>MΩ</td>
<td>Megohm or $10^6 \Omega$</td>
</tr>
<tr>
<td>mA</td>
<td>Milliampere or $10^{-3} A$</td>
</tr>
<tr>
<td>max.</td>
<td>Maximum</td>
</tr>
<tr>
<td>MHz</td>
<td>Megahertz or $10^6 Hz$</td>
</tr>
<tr>
<td>min.</td>
<td>Minimum</td>
</tr>
<tr>
<td>mm</td>
<td>Millimeter or $10^{-3} m$</td>
</tr>
<tr>
<td>LT</td>
<td>Lower tester</td>
</tr>
<tr>
<td>N</td>
<td>Newton</td>
</tr>
<tr>
<td>NAD</td>
<td>Node Address</td>
</tr>
<tr>
<td>NAK</td>
<td>Negative Acknowledgment</td>
</tr>
<tr>
<td>ns</td>
<td>Nanosecond or $10^{-9} s$</td>
</tr>
<tr>
<td>P1</td>
<td>Parameter 1</td>
</tr>
<tr>
<td>P2</td>
<td>Parameter 2</td>
</tr>
<tr>
<td>P3</td>
<td>Parameter 3</td>
</tr>
<tr>
<td>PCB</td>
<td>Protocol Control Byte</td>
</tr>
<tr>
<td>PCO</td>
<td>Point of Control and Observation</td>
</tr>
<tr>
<td>pF</td>
<td>Picofarad or $10^{-12} F$</td>
</tr>
<tr>
<td>R-APDU</td>
<td>Response APDU</td>
</tr>
<tr>
<td>R-block</td>
<td>Receive Ready Block</td>
</tr>
<tr>
<td>RH</td>
<td>Relative Humidity</td>
</tr>
<tr>
<td>RST</td>
<td>Reset</td>
</tr>
<tr>
<td>R-TPDU</td>
<td>Response TPDU</td>
</tr>
<tr>
<td>S-block</td>
<td>Supervisory Block</td>
</tr>
<tr>
<td>SI</td>
<td>International System of Units Standard</td>
</tr>
<tr>
<td>SUT</td>
<td>System Under Test</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>SW1</td>
<td>Status Word 1</td>
</tr>
<tr>
<td>SW2</td>
<td>Status Word 2</td>
</tr>
<tr>
<td>TCK</td>
<td>Check Character</td>
</tr>
<tr>
<td>t_F</td>
<td>Fall Time Between 90% and 10% of Signal Amplitude</td>
</tr>
<tr>
<td>TPDU</td>
<td>Transport Protocol Data Unit</td>
</tr>
<tr>
<td>t_R</td>
<td>Rise Time Between 10% and 90% of Signal Amplitude</td>
</tr>
<tr>
<td>TTL</td>
<td>Terminal Transport Layer</td>
</tr>
<tr>
<td>UT</td>
<td>Upper Tester</td>
</tr>
<tr>
<td>V</td>
<td>Volt</td>
</tr>
<tr>
<td>V_CC</td>
<td>Voltage Measured between VCC and GND Contacts</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>V_H</td>
<td>High Level Input Voltage</td>
</tr>
<tr>
<td>V_L</td>
<td>Low Level Input Voltage</td>
</tr>
<tr>
<td>V_OH</td>
<td>High Level Output Voltage</td>
</tr>
<tr>
<td>V_OL</td>
<td>Low Level Output Voltage</td>
</tr>
<tr>
<td>Vpp</td>
<td>Volts Peak to Peak</td>
</tr>
<tr>
<td>VPP</td>
<td>Programming Voltage</td>
</tr>
<tr>
<td>WI</td>
<td>Waiting Time Integer</td>
</tr>
<tr>
<td>WTX</td>
<td>Waiting Time Extension</td>
</tr>
</tbody>
</table>

All units in this document follow the International System of Units (SI) standard.
3.2 Definitions

In addition of terms already defined in the reference documentation, the following terms are used in this document:

- **Acceptance Testing**: Set of procedures and tests to perform for the qualification of a Test Tool or Test Bench.

- **Protocol Tests**: A defined set of test that checks the software responsible for the data exchange between ICC and IFM.

- **Sample**: A physical implementation of an ICC or an IFM (design), delivered to the Testing Laboratory for the test.

- **Test Bench**: A system designed to perform the Test Cases described in this document.

- **Test Case**: A test to verify a defined subset of the requirements under specific test conditions.

- **Test Code**: The code identifying a Test Case.

- **Testing Laboratory**: A facility accredited by EMVCo for performing EMV Type Approval testing of IFMs.

- **Transaction**: A sequence of logic interactions that the ICC and the Terminal shall execute as foreseen by the EMV application.

- **Trigger delay**: Property of a digitizing circuit to not follow immediately the input signal changes that are shorter than the Trigger Delay, so that less switching is generated.
4 General requirements

4.1 Testing Strategy

4.1.1 Compliance Demonstration Objective

Within EMVCo Level 1 type approval process, EMVCo compliance demonstration objectives are:
1. To ensure implementation of the EMVCo Book 1 requirements (see [D01]);
2. To ensure that ICC and Terminal do not damage one another;
3. To ensure ICC / Terminal interoperability whatever the terminal customization performed by the vendor.

4.1.2 Device Under Test for Level 1 Approval.

The DUT is the Interface Module (IFM) as defined in the “Terminal Level 1 Type Approval - Administrative Process” document (See [D05]).

4.2 Test Tool Implementation Requirements

4.2.1 Physical compatibility requirements

The physical compatibility shall be verified by using probes that are dimensionally calibrated. The first probe has minimum dimensions and the second has maximum dimensions.

The «Minimum dimensions probe» shall have the following size :
- Length = 85.47 mm ± 80 µm
- Width = 53.92 mm ± 80 µm
- Thickness = 680 µm ± 40 µm for the card surface
  680 µm ± 60 µm for the contacting areas
  680 µm ± 100 µm for the probe connectors zone located outside of the ISO card surface
- Radius (card corners) = 3.18 mm ± 0.3 mm
- Radius (card thickness) ≤ 0.15 mm
- Specific dimensions (to be described in the Tool documentation) : a, b and c.
The layout (top view) of the minimum dimensions probe shall be as follows:

![Top view diagram](image)

Figure 1 – Top view of the minimum dimensions probe

The cross-section (side view) of the minimum dimensions probe shall be as follows:

![Side view diagram](image)

Figure 2 – Side view of the minimum dimensions probe

The «Maximum dimensions probe» shall have the following size:

- Length = 85.90 mm +0 - 80 µm
- Width = 54.18 mm +0 - 80 µm
- Thickness = 840 µm +40 +0 µm for the card surface
  - 840 µm +60 +0 µm for the contacting areas
  - 1350 µm +80 +0 µm for the embossing areas (Card number area, name and address area)
  - 840 µm ± 100 µm for the probe connectors zone located outside of the ISO card surface
- Radius (card corners) = 3.18 mm ± 0.3 mm
- Radius (card thickness) ≤ 0.15 mm
- Specific dimensions (to be described in the Tool documentation) : a, b and c.
The layout (top view) of the maximum dimensions probe shall be as follows:

![Top view](image)

**Figure 3 – Top view of the maximum dimensions probe**

The cross-section (side view) of the maximum dimensions probe shall be as follows:

![Side view](image)

**Figure 4 – Side view of the maximum dimensions probe**
The contacts locations and dimensions for both probes shall be the minimum contact size that is allowed by ISO 7816-2. The test probes contact pads dimensional tolerance allowed is ±0 +40 µm in length or width, measured from the center of the pad and based on the ‘ISO minimal contacts’ definition, as shown below:

![Diagram showing contact pad dimensions](image)

**Figure 5 – Top view of a contact pad for both probes**

### 4.2.2 Contact forces requirements

The contact forces shall be verified by using a probe that is calibrated for its dimensions as well as its capabilities to measure the forces that the DUT exerts on each individual contact.

The «Contact forces measurement probe» shall have the following size:

- Length = 85.72 mm ±40 µm
- Width = 54.03 mm ±40 µm
- Thickness = 760 µm ±0 +40 µm
- Radius (card corners) = 3.18 mm ± 0.3 mm
- Radius (card thickness) ≤ 0.15 mm

The ISO minimum window must be located completely inside the measurement window.

The contact forces measurement probe shall be able to measure contact forces from 0.0 N to 1.0 N with a measurement uncertainty of ± 0.15 N for each contact. The influence of neighboring contact forces on any measurement shall be as minimized as possible.

During contact force measurements, the contact force measuring device surface shall not move along the force axis by more than +20 ·80 µm from its nominal surface position when sustaining IFM contact forces ranging from 0.0 N to 0.8 N.

The probe used for the contact force measurement shall not apply more torque than a normal card.
4.2.3 Electrical signal generation requirements

The Test Bench shall be capable of generating the signals needed to conduct appropriately the Test Cases listed below. This means that the Test Bench shall be capable of driving the contacts listed below for the ranges specified, with the corresponding uncertainties (or better), as follows:

<table>
<thead>
<tr>
<th>Contact</th>
<th>Parameter</th>
<th>Range or value</th>
<th>Uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>ICLK</td>
<td>-49 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+10 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+49 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td>I/O</td>
<td>IO</td>
<td>-495 μA</td>
<td>± 2.5 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-5 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+5 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td>Rise and fall times</td>
<td>≤ 100 ns</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1075 ns</td>
<td>± 125 ns</td>
</tr>
<tr>
<td></td>
<td>VOL</td>
<td>0.0 V DC</td>
<td>± 30 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5 V DC</td>
<td>± 30 mV</td>
</tr>
<tr>
<td></td>
<td>VOH</td>
<td>0.6 × VCC</td>
<td>± 30 mV (1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCC</td>
<td>± 30 mV (2)</td>
</tr>
<tr>
<td>RST</td>
<td>IRST</td>
<td>-49 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+10 μA</td>
<td>± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+49 μA</td>
<td>± 1 μA</td>
</tr>
</tbody>
</table>

(1) This uncertainty includes the related VCC measurement uncertainty.
(2) This uncertainty includes the related VCC measurement uncertainty.
All contacts except VCC shall present a capacitance less than or equal to 30 pF.

### 4.2.4 Electrical measurement requirements

The Test Bench shall be capable of measuring the signals needed to perform appropriately the Test Cases listed below. This means that the Test Bench shall be capable of measuring the parameters of the contacts listed below for the ranges specified, with the corresponding uncertainties (or better), as follows:

<table>
<thead>
<tr>
<th>Contact</th>
<th>Parameter</th>
<th>Range</th>
<th>Uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Duty cycle</td>
<td>30% to 70%</td>
<td>± 1%</td>
</tr>
<tr>
<td></td>
<td>Frequency</td>
<td>0.1 MHz to 6.0 MHz</td>
<td>± 1%</td>
</tr>
<tr>
<td></td>
<td>Rise and fall times</td>
<td>0 ns to 1000 ns</td>
<td>± 5% ± 2ns</td>
</tr>
<tr>
<td></td>
<td>1000 ns to 2000 ns</td>
<td>± 125 ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Voltage to GND</td>
<td>±1 V DC to 6 V DC</td>
<td>± 15 mV</td>
</tr>
<tr>
<td></td>
<td>Voltage compared to Vcc</td>
<td>±1 V DC to 6 V DC</td>
<td>± 25 mV</td>
</tr>
<tr>
<td>Contact</td>
<td>Parameter</td>
<td>Range</td>
<td>Uncertainty</td>
</tr>
<tr>
<td>---------</td>
<td>-----------------------------------</td>
<td>------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>I/O</td>
<td>$I_{IO}$</td>
<td>-20 mA to +20 mA</td>
<td>± 0.1 mA</td>
</tr>
<tr>
<td></td>
<td>Rise and fall times</td>
<td>0 ns to 1000 ns</td>
<td>± 50 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000 ns to 2000 ns</td>
<td>± 125 ns</td>
</tr>
<tr>
<td></td>
<td>Voltage to GND</td>
<td>-1 V DC to 6 V DC</td>
<td>± 15 mV</td>
</tr>
<tr>
<td></td>
<td>Voltage compared to $V_{CC}$</td>
<td>-1 V DC to 6 V DC</td>
<td>± 25 mV</td>
</tr>
<tr>
<td>RST</td>
<td>Rise and fall times</td>
<td>0 ns to 1000 ns</td>
<td>± 50 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000 ns to 2000 ns</td>
<td>± 125 ns</td>
</tr>
<tr>
<td></td>
<td>Voltage to GND</td>
<td>-1 V DC to 6 V DC</td>
<td>± 15 mV</td>
</tr>
<tr>
<td></td>
<td>Voltage compared to $V_{CC}$</td>
<td>-1 V DC to 6 V DC</td>
<td>± 25 mV</td>
</tr>
<tr>
<td>VCC</td>
<td>Voltage to GND</td>
<td>-1 V DC to 6 V DC</td>
<td>± 15 mV</td>
</tr>
<tr>
<td>VPP</td>
<td>Resistance to GND</td>
<td>0.1 MΩ to 20 MΩ</td>
<td>± 5%</td>
</tr>
<tr>
<td></td>
<td>Voltage to GND</td>
<td>-1 V DC to 6 V DC</td>
<td>± 15 mV</td>
</tr>
</tbody>
</table>

Table 2 – Electrical signal measurement requirements

All contacts shall be protected such as to withstand contact voltages ranging from -10 V DC to +25 V DC with a maximum input current of ± 20 mA without any damage for the Test Bench.
4.2.5 Environmental monitoring requirements

The Laboratory shall be capable of measuring the environmental conditions enforced around the IFM during the Test Cases, as listed below. This means that the Test Bench shall be capable of measuring the parameters listed below in the Laboratory room and/or the climatic chamber for the ranges specified, with the corresponding uncertainties (or better), as follows:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>0°C to 50°C</td>
<td>± 1°C</td>
</tr>
<tr>
<td>Relative Humidity</td>
<td>5% RH to 95% RH</td>
<td>± 3% RH</td>
</tr>
</tbody>
</table>

Table 3 – Environmental monitoring requirements

4.3 Test Conditions

4.3.1 Default environmental conditions

Each Electrical and Card Session Type Approval test shall be performed under the following environmental conditions:

<table>
<thead>
<tr>
<th>Condition</th>
<th>Temperature</th>
<th>Relative humidity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low temperature</td>
<td>6°C ± 1°C</td>
<td>50% RH ± 10% RH</td>
</tr>
<tr>
<td>Normal temperature</td>
<td>23°C ± 3°C</td>
<td>50% RH ± 10% RH</td>
</tr>
<tr>
<td>High temperature</td>
<td>39°C ± 1°C</td>
<td>50% RH ± 10% RH</td>
</tr>
</tbody>
</table>

Table 4 – Type Approval Tests environmental conditions

4.3.2 ATR

Unless specified otherwise in the Test Cases below, the default T=0 ATR shall be used. For details on the ATR used, please refer to document [D06].

4.3.3 Loopback

The transactions needed to perform the Test Cases described below rely on a specific application called “Loopback”. For a description of this application, please refer to the document [D07].
4.3.4 Test Case Naming Convention

The Test Cases References are established as follows:

1Ct.nnn.cc

where

1C stands contact terminal level 1 test case

t is a letter indicating the category of test case

nnn is a the number of the test case

cc is the number of the test sub-case, or 00 if there is no sub-case
5 Mechanical Test Cases

5.1 1CA.001.0x - Physical compatibility and contact location

This test verifies that the physical characteristics of the DUT allow the acceptance of ICCs having a size between the standard minimum and the maximum dimensions, and that galvanic contact is established between the DUT and ICCs having minimal area contacts.

Test Code
1CA.001.0x

Reference
This test refers to requirements in [D01], section 5.4.1.

Test Conditions
Use Table 5 for the test conditions during verifications of the physical compatibility and contact location.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Reference probe to be used</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Minimum dimensions</td>
</tr>
<tr>
<td>2</td>
<td>Maximum dimensions</td>
</tr>
</tbody>
</table>

Table 5 – Test conditions for 1CA.001.0x

Procedure
Follow this procedure to verify the physical compatibility and contact location:
1. Stabilize the DUT at normal temperature.
2. Insert the reference probe listed in the first line of Table 5 into the DUT.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of one second.
5. Withdraw the reference probe from the DUT.
6. Using the reference probe listed in the second line of Table 5, repeat steps 3 to 5.

Acceptance criteria
The following acceptance criteria shall be met under all test conditions:
1. The reference probes may be inserted without mechanical interference into the DUT.
2. The contact activation sequence and the processing of the command sequence between the Test Bench and IUT are correctly performed.
3. The reference probes may be withdrawn from the DUT without mechanical interference.

**Expected Results**

Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
5.2 1CA.002.00 – IFM Contact Forces

This test verifies that the force exerted by any one DUT contact over its corresponding ICC contact is within specifications.

Test Code
1CA.002.00

Reference
This test refers to requirements in [D01], section 5.4.2.

Test Conditions
The DUT is not supplied any power.

Procedure
Follow this procedure to verify the IFM contact forces:
1. Stabilize the DUT at normal temperature.
2. Insert the contact force measuring probe into the DUT, up to its nominal seated position. Position the probe so as to avoid any perturbations during the measurement.
3. Measure the force on each existing contact pad at least three times with at least one second between measurements.
4. Withdraw the contact forces measuring probe from the DUT.

Acceptance criteria
The following acceptance criteria shall be met for each contact:
1. $(0.2 \text{ N} - \varepsilon \text{N}) \leq \text{contact force} \leq (0.6 \text{ N} + \varepsilon \text{N})$

The “contact force” mentioned in the Acceptance Criteria 1 above is the average of the three measurements performed on the concerned contact.

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6 Electrical Test Cases

6.1 Foreword

This section describes the general conditions for all electrical and card session test cases. The indications below are applicable to all the test cases, unless otherwise is stated in the description of a specific test case.

The monitoring of the signals shall start the first time that VCC reaches its lowest stable limit, i.e. (4.6 V DC - εV) for Class A or (2.76 V - εV) for Class B, and end when VCC is deactivated.

Regarding signal voltages, a differentiated approach has been selected:

- The “Signal voltage” series of test cases focus on the general DC shape of the signals. Shortest spikes, i.e. those lasting less than the “Trigger delay” value, are ignored. For these test cases:
  - All acceptance limits are set according to the requirements applicable to the IFM.
  - Appropriate trigger delays are applied. Spikes shorter than the concerned trigger delay are ignored.
  - To accommodate for the unavoidable internal resistance of the transmission lines, the outer voltage limits, i.e. the lower VIL limit and the upper VIH limit, are shifted by 50mV from their nominal specified value.

- The “Signal perturbations” series of test cases focus on the high-frequency components of the signal, and on ensuring that the signals are appropriate for interpretation by the ICC. For these test cases:
  - No trigger delay is applied. A spike that is outside limits results in a failed test case, whatever its duration.
  - The outer limits, i.e. the lower VIL limit and the upper VIH limit, are verified against the “Signal perturbations” IFM specifications.
  - The inner limits, i.e. the lower VIH limit and the upper VIL limit, are verified against the ICC receiver specifications.
  - The correct signals transitions, i.e. from low to high state and vice-versa, are verified.

The ICC current specified in each test condition shall be driven by the Test Tool from the moment when VCC is powered up and stable until its deactivation.
6.2 1CB.001.0x - Short circuit resilience

This test verifies that the DUT is not damaged by a short circuit between any pair or group of contacts.

Test Code
1CB.001.0x

Reference
This test refers to requirements in [D01], section 5.5.8.

Test Conditions
Use Table 6 for the test conditions during verifications of the short circuit resilience.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Probe description</th>
<th>$I_{cc}$ ($^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Shorts I/O, CLK and RST to GND with $\leq 2\Omega$ each</td>
<td>$2 \text{ mA } \pm 2% \pm 0.1 \text{ mA}$</td>
</tr>
<tr>
<td>2</td>
<td>Shorts I/O, CLK and RST to VCC with $\leq 2\Omega$ each</td>
<td>$2 \text{ mA } \pm 2% \pm 0.1 \text{ mA}$</td>
</tr>
<tr>
<td>3</td>
<td>Shorts VCC to GND with $\leq 2\Omega$</td>
<td>$54 \text{ mA } \pm 2% \pm 0.1 \text{ mA}$</td>
</tr>
<tr>
<td>4</td>
<td>Fully metallic probe with $\leq 2\Omega$ between any pair of contacts, or between any contact and any point of the surface of the probe.</td>
<td>$54 \text{ mA } \pm 2% \pm 0.1 \text{ mA}$</td>
</tr>
</tbody>
</table>

Table 6 – Test conditions for 1CB.001.0x

Procedure

Follow this procedure to verify the short circuit resilience:
1. Stabilize the DUT at normal temperature.
2. Insert the reference probe listed in the first line of Table 6 into the DUT.
3. Keep the probe inserted for at least 10 seconds.
4. Withdraw the reference probe.
5. If required by the DUT operating instructions, perform a reset of the DUT.
6. Insert the normal measurement probe and initiate cold reset.
7. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
8. During step 7, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND), the I/O voltage between contacts C7 (I/O) and C5 (GND) when the DUT is transmitting, the CLK voltage between contacts C3 (CLK) and C5 (GND) and the RST voltage between contacts C2 (RST) and C5 (GND).
9. Use the reference probe listed in the next line of Table 6 and repeat steps 2 to 8. Repeat this step until the end of the table.

($^3$) This current applies to the transaction performed after each short (steps 6, 7 and 8), not during the shorts (steps 2 and 3).
Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all test conditions:

1. Each sequence of commands and answers in step 7 of the procedure above is performed correctly.

2. 
   
   \[-0.25 \text{ V} \cdot \varepsilon \text{V} \leq \text{Low state I/O voltage} \leq ((0.15 \times \text{V}_{\text{CC}}) + \varepsilon \text{V})\]

3. 
   
   \[(0.8 \times \text{V}_{\text{CC}}) \cdot \varepsilon \text{VV} \leq \text{High state I/O voltage} \leq (\text{V}_{\text{CC}} + 0.25 \text{ V} + \varepsilon \text{VV})\]

4. 
   
   \[-0.25 \text{ V} \cdot \varepsilon \text{V} \leq \text{Low state CLK voltage} \leq ((0.15 \times \text{V}_{\text{CC}}) + \varepsilon \text{VV})\]

5. 
   
   \[(0.8 \times \text{V}_{\text{CC}}) \cdot \varepsilon \text{VV} \leq \text{High state CLK voltage} \leq (\text{V}_{\text{CC}} + 0.25 \text{ V} + \varepsilon \text{VV})\]

6. 
   
   \[-0.25 \text{ V} \cdot \varepsilon \text{V} \leq \text{Low state RST voltage} \leq ((0.15 \times \text{V}_{\text{CC}}) + \varepsilon \text{VV})\]

7. 
   
   \[(0.8 \times \text{V}_{\text{CC}}) \cdot \varepsilon \text{VV} \leq \text{High state RST voltage} \leq (\text{V}_{\text{CC}} + 0.25 \text{ V} + \varepsilon \text{VV})\]

8. 
   
   \[-0.25 \text{ V} \cdot \varepsilon \text{V} \leq \text{V}_{\text{CC}} \text{ voltage (at any time)}\]

9. For Class A:
   a. \[-0.25 \text{ V} \cdot \varepsilon \text{V} \leq \text{V}_{\text{CC}} \text{ voltage} \leq (5.40 \text{ V} + \varepsilon \text{V})\]
   b. When CLK is active : \((4.60 \text{ V} \cdot \varepsilon \text{V}) \leq \text{V}_{\text{CC}} \text{ voltage}\)

10. For Class B:
   a. \[-0.25 \text{ V} \cdot \varepsilon \text{V} \leq \text{V}_{\text{CC}} \text{ voltage} \leq (3.24 \text{ V} + \varepsilon \text{V})\]
   b. When CLK is active : \((2.76 \text{ V} \cdot \varepsilon \text{V}) \leq \text{V}_{\text{CC}} \text{ voltage}\)

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.3 1CB.002.00 - VPP isolation

This test verifies the isolation of the VPP contact for new IFM designs.
This test case is applicable to all Class B DUTs and to Class A DUTs when their ICS mentions that the VPP contact (C6) is not connected. For other Class A DUTs, please perform the test case 1CB.003.0x instead.

Test Code
1CB.002.0x

Reference
This test refers to requirements in [D01], section 5.5.3.

Test Conditions
No specific test conditions are applicable to this test case.

Procedure
Follow this procedure to verify the isolation of the VPP contact for new IFM designs:
1. Stabilize the DUT at normal temperature.
2. Initiate cold reset.
3. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
4. During step 3, measure the DC resistance between contacts C6 (VPP) and C5 (GND). The test voltage used shall not exceed 5 V DC between these contacts.

Acceptance criteria
The following acceptance criteria shall be met:
1. VPP isolation ≥ (10 MΩ · εΩ)

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.4 1CB.003.0x - VPP voltage

This test verifies the voltage on the VPP contact for existing Class A IFM designs.

This test case is applicable only to existing Class A DUTs, when their ICS mentions that the VPP contact (C6) is connected. For all other DUTs, please perform the test case 1CB.002.00 instead.

Test Code
1CB.003.0x

Reference
This test refers to requirements in [D01], section 5.5.3.

Test Conditions
Use Table 7 for the test conditions during verifications of the voltage on the VPP contact for existing Class A IFM designs.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Icc</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( \leq 0.2 \text{ mA} )</td>
</tr>
<tr>
<td>2</td>
<td>2 mA ( \pm 2% \pm 0.1 \text{ mA} )</td>
</tr>
<tr>
<td>3</td>
<td>54 mA ( \pm 2% \pm 0.1 \text{ mA} )</td>
</tr>
</tbody>
</table>

Table 7 – Test conditions for 1CB.003.0x

Procedure
Follow this procedure to verify the voltage on the VPP contact for existing Class A IFM designs:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 7.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During steps 3 and 4, monitor the VPP voltage between contacts C6 (VPP) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 7 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. \((-0.25 \text{ V} \cdot \epsilon \text{V}) \leq \text{VPP voltage} \leq ((1.05 \times V_{CC}) + 0.25 \text{ V DC} + \epsilon \text{VV})\)
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.5 1CB.004.0x - I/O current

This test verifies the current limitation on the I/O contact.

Test Code
1CB.004.0x

Reference
This test refers to requirements in [D01], section 5.5.2.

Test Conditions
Use Table 8 for the test conditions during verifications of the current limitation on the I/O contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>$I_{CC}$</th>
<th>Shorting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA $\pm$ 2% $\pm$ 0.1 mA</td>
<td>$\leq 75\Omega$ from I/O to VCC</td>
</tr>
<tr>
<td>2</td>
<td>54 mA $\pm$ 2% $\pm$ 0.1 mA</td>
<td>$\leq 75\Omega$ from I/O to VCC</td>
</tr>
<tr>
<td>3</td>
<td>2 mA $\pm$ 2% $\pm$ 0.1 mA</td>
<td>$\leq 75\Omega$ from I/O to GND</td>
</tr>
<tr>
<td>4</td>
<td>54 mA $\pm$ 2% $\pm$ 0.1 mA</td>
<td>$\leq 75\Omega$ from I/O to GND</td>
</tr>
</tbody>
</table>

Table 8 – Test conditions for 1CB.004.0x

Procedure
Follow this procedure to verify the current limitation on the I/O contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the “$I_{CC}$” column of the first line of Table 8.
3. Initiate cold reset.
4. Send the default T=0 ATR without any short circuit.
5. When the DUT sends data to the LT, apply the short circuit specified in the “Shorting” column of the concerned line of Table 8 until the short collapses I/O and cause contact deactivation, or after one second.
6. During step 5, monitor the I/O current on contact C7 (I/O) starting 100 ns after the application of the short circuit.
7. Set the test conditions as listed in the next line of Table 8 and repeat steps 3 to 6. Repeat this step until the end of the table.
8. Repeat steps 1 to 7 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:
1. $(15\ mA \cdot \varepsilon A) \leq I/O \ \text{current} \leq (15\ mA + \varepsilon A)$
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.6 1CB.005.0x - I/O transmission voltage

This test verifies the voltage trends on the I/O contact when the DUT is transmitting, i.e. when the DUT is controlling the level on the I/O contact.

**Test Code**

1CB.005.0x

**Reference**

This test refers to requirements in [D01], section 5.5.2.1, Table 10.

**Test Conditions**

Use Table 9 for the test conditions during verifications of the voltage trends on the I/O contact during transmission.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>I$_{CC}$</th>
<th>I$_{IO}$</th>
<th>Trigger delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA, -495 μA ± 2.5 μA</td>
<td>320 ns</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA, -495 μA ± 2.5 μA</td>
<td>320 ns</td>
</tr>
</tbody>
</table>

**Table 9 – Test conditions for 1CB.005.0x**

**Procedure**

Follow this procedure to verify the voltage trends on the I/O contact during transmission:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 9.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the I/O voltage between contacts C7 (I/O) and C5 (GND) when the DUT is transmitting.
6. Set the test conditions as listed in the next line of Table 9 and repeat steps 3 to 5.
7. Repeat steps 1 to 6 for all other environmental conditions.

**Acceptance criteria**

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. (-50 mV - εV) ≤ Low state I/O voltage ≤ ((0.15 × V$_{CC}$) + εVV)
2. ((0.8 × V$_{CC}$) - εVV) ≤ High state I/O voltage ≤ (V$_{CC}$ + 50 mV + εVV)

To be recognized as a failed test, a non-compliance situation shall last at least for the trigger delay duration.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.7 1CB.006.0x - I/O transmission rise and fall time

This test verifies the rise and fall times on the I/O contact when the DUT is transmitting, i.e. when the DUT is controlling the level on the I/O contact.

Test Code
1CB.006.0x

Reference
This test refers to requirements in [D01], section 5.5.2.1, Table 10.

Test Conditions
Use Table 10 for the test conditions during verifications of the rise and fall times on the I/O contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Icc</th>
<th>Io</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA ±5 μA ± 1 μA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA ±5 μA ± 1 μA</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA 495 μA ± 2.5 μA</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA 495 μA ± 2.5 μA</td>
</tr>
</tbody>
</table>

Table 10 – Test conditions for 1CB.006.0x

Procedure
Follow this procedure to verify the rise and fall times on the I/O contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 10.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the I/O rise time (10% to 90% of (0.2 × Vcc) to (0.7 × Vcc)) and the I/O fall time (90% to 10% of (0.7 × Vcc) to (0.2 × Vcc)) between contacts C7 (I/O) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 10 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.
Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. I/O rise time ≤ (800 ns + εs)
2. I/O fall time ≤ (800 ns + εs)

Expected Results
Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.8 1CB.007.0x - I/O transmission signal perturbations

This test verifies the voltage perturbations on the I/O contact when the DUT is transmitting, i.e. when the DUT is controlling the level on the I/O contact.

Test Code
1CB.007.0x

Reference
This test refers to requirements in [D01], section 5.5.2.1, Table 10.

Test Conditions
Use Table 11 for the test conditions during verifications of the voltage perturbations on the I/O contact during transmission.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>ICC</th>
<th>IIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+5 μA ± 1 μA</td>
</tr>
</tbody>
</table>

Table 11 – Test conditions for 1CB.007.0x

Procedure
Follow this procedure to verify the voltage perturbations on the I/O contact during transmission:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 11.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the I/O voltage between contacts C7 (I/O) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 11 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.
Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. \((-0.25 \, \text{V} \cdot \varepsilon \text{V}) \leq \text{I/O voltage} \leq (V_{CC} + 0.25 \, \text{V} + \varepsilon \text{V})\)

2. Each time that the I/O voltage increases over \((0.2 \times V_{CC}) + \varepsilon \text{VV}\), it reaches next \((0.7 \times V_{CC}) - \varepsilon \text{V}\) or above before decreasing again under \((0.2 \times V_{CC}) + \varepsilon \text{VV}\). To avoid inappropriate detection of failures in open-drain IFM implementations, the two first clock cycles after each state transition shall be ignored.

3. Each time that the I/O voltage decreases under \((0.7 \times V_{CC}) - \varepsilon \text{V}\), it reaches next \((0.2 \times V_{CC}) + \varepsilon \text{VV}\) or below before increasing again over \((0.7 \times V_{CC}) - \varepsilon \text{V}\).

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.9 1CB.008.0x - I/O reception voltage

This test verifies that the DUT is able to correctly interpret the signal from an ICC that generates I/O voltages which are on the boundaries of the acceptable voltage specifications.

Test Code
1CB.008.0x

Reference
This test refers to requirements in [D01], section 5.5.2.2, Table 11.

Test Conditions
Use Table 12 for the test conditions during verifications of the signal voltage interpretation on the I/O contact during reception.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>I_{CC}</th>
<th>I/O V_OL</th>
<th>I/O V_OH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA± 2% ± 0.1 mA</td>
<td>0.0 V DC ± 30 mV</td>
<td>V_{CC} ± 30 mV</td>
</tr>
<tr>
<td>2</td>
<td>54 mA± 2% ± 0.1 mA</td>
<td>0.0 V DC ± 30 mV</td>
<td>V_{CC} ± 30 mV</td>
</tr>
<tr>
<td>3</td>
<td>2 mA± 2% ± 0.1 mA</td>
<td>(0.2 \times V_{CC}) - 30 mV ± 30 mV</td>
<td>(0.6 \times V_{CC}) + 30 mV ± 30 mV</td>
</tr>
<tr>
<td>4</td>
<td>54 mA± 2% ± 0.1 mA</td>
<td>(0.2 \times V_{CC}) - 30 mV ± 30 mV</td>
<td>(0.6 \times V_{CC}) + 30 mV ± 30 mV</td>
</tr>
</tbody>
</table>

Table 12 – Test conditions for 1CB.008.0x

When generated by the Test Bench, the rise and fall times of the I/O signal shall be less than or equal to 100 ns of the concerned V\_OL to V\_OH range.

Procedure
Follow this procedure to verify the signal voltage interpretation on the I/O contact during reception:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 12.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. Set the test conditions as listed in the next line of Table 12 and repeat steps 3 and 4. Repeat this step until the end of the table.
6. Repeat steps 1 to 5 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. Each sequence of commands and answers is performed correctly.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.10 1CB.009.0x - I/O reception rise and fall times

This test verifies that the DUT is able to correctly interpret the signal from an ICC that generates rise and fall times which are on the boundaries of the acceptable timing specifications.

Test Code
1CB.009.0x

Reference
This test refers to requirements in [D01], section 5.5.2.2, Table 11.

Test Conditions
Use Table 13 for the test conditions during verifications of the signal rise and fall times interpretation on the I/O contact during reception.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>$I_{CC}$</th>
<th>I/O $t_R$ and $t_F$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>≤ 100 ns</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>≤ 100 ns</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>1075 ns ± 125 ns</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>1075 ns ± 125 ns</td>
</tr>
</tbody>
</table>

Table 13 – Test conditions for 1CB.009.0x

When generated by the Test Bench, the voltages of the I/O signal shall be as follows:
- I/O $V_{OL} = 0.0$ V DC ± 30 mV
- I/O $V_{OH} = V_{CC} ± 30$ mV if controlled by the Test Tool, else floating
- The rise time is 10% to 90% of 0.0 V DC to $V_{CC}$
- The fall time is 90% to 10% of $V_{CC}$ to 0.0 V DC

Procedure
Follow this procedure to verify the signal rise and fall times interpretation on the I/O contact during reception:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 13.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. Set the test conditions as listed in the next line of Table 13 and repeat steps 3 and 4. Repeat this step until the end of the table.
6. Repeat steps 1 to 5 for all other environmental conditions.
Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. Each sequence of commands and answers is performed correctly.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.11 1CB.010.0x - CLK voltage

This test verifies the voltage trends on the CLK contact.

**Test Code**

1CB.010.0x

**Reference**

This test refers to requirements in [D01], section 5.5.4, Table 12.

**Test Conditions**

Use Table 14 for the test conditions during verifications of the voltage trends on the CLK contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>I\textsubscript{CC}</th>
<th>I\textsubscript{CLK}</th>
<th>Trigger delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA</td>
<td>60 ns</td>
</tr>
<tr>
<td></td>
<td>-49 μA ± 1 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA</td>
<td>60 ns</td>
</tr>
<tr>
<td></td>
<td>-49 μA ± 1 μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Table 14 – Test conditions for 1CB.010.0x*

**Procedure**

Follow this procedure to verify the voltage trends on the CLK contact:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 14.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK voltage between contacts C3 (CLK) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 14 and repeat steps 3 to 5.
7. Repeat steps 1 to 6 for all other environmental conditions.

**Acceptance criteria**

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. \((-50 \text{ mV} \cdot e\text{V}) \leq \text{Low state CLK voltage} \leq ((0.15 \times V_{CC}) + e\text{VV})\)
2. \(((0.8 \times V_{CC}) \cdot e\text{VV}) \leq \text{High state CLK voltage} \leq (V_{CC} + 50 \text{ mV} + e\text{VV})\)

To be recognized as a failed test, a non-compliance situation shall last at least for the trigger delay duration.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.12 1CB.011.0x - CLK rise and fall times

This test verifies the rise and fall times on the CLK contact.

Test Code
1CB.011.0x

Reference
This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions
Use Table 15 for the test conditions during verifications of the rise and fall times on the CLK contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>( I_{CC} )</th>
<th>( I_{CLK} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA (-10 \mu \text{A} ± 1 \mu \text{A})</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA (-10 \mu \text{A} ± 1 \mu \text{A})</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA (-49 \mu \text{A} ± 1 \mu \text{A})</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA (-49 \mu \text{A} ± 1 \mu \text{A})</td>
</tr>
</tbody>
</table>

Table 15 – Test conditions for 1CB.011.0x

Procedure
Follow this procedure to verify the rise and fall times on the CLK contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 15.
3. Initiate cold reset.
4. Send the default \( T=0 \) ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK rise time (10% to 90% of \( 0.2 \times V_{CC} \)) to \( (0.7 \times V_{CC}) \) and the CLK fall time (90% to 10% of \( 0.7 \times V_{CC} \)) to \( (0.2 \times V_{CC}) \) between contacts C3 (CLK) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 15 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.
Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. CLK rise time ≤ (8% of clock period + εs)
2. CLK fall time ≤ (8% of clock period + εs)

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.13 1CB.012.0x - CLK signal perturbations

This test verifies the voltage perturbations on the CLK contact.

Test Code
1CB.012.0x

Reference
This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions
Use Table 16 for the test conditions during verifications of the voltage perturbations on the CLK contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>ICC</th>
<th>ICLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA +10 μA ± 1 μA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA +10 μA ± 1 μA</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA +49 μA ± 1 μA</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA +49 μA ± 1 μA</td>
</tr>
</tbody>
</table>

Table 16 – Test conditions for 1CB.012.0x

Procedure
Follow this procedure to verify the voltage perturbations on the CLK contact:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 16.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK voltage between contacts C3 (CLK) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 16 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.
Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. \((-0.25 \, \text{V} \pm \epsilon \text{V}) \leq \text{CLK voltage} \leq (\text{V}_{\text{CC}} + 0.25 \, \text{V} + \epsilon \text{V})\)

2. Each time that the CLK voltage increases over \(((0.2 \times \text{V}_{\text{CC}}) + \epsilon \text{V})\), it reaches next \(((0.7 \times \text{V}_{\text{CC}}) - \epsilon \text{V})\) or above before decreasing again under \(((0.2 \times \text{V}_{\text{CC}}) + \epsilon \text{V})\).

3. Each time that the CLK voltage decreases under \(((0.7 \times \text{V}_{\text{CC}}) - \epsilon \text{V})\), it reaches next \(((0.2 \times \text{V}_{\text{CC}}) + \epsilon \text{V})\) or below before increasing again over \(((0.7 \times \text{V}_{\text{CC}}) - \epsilon \text{V})\).

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.14 1CB.013.0x - CLK frequency and duty cycle

This test verifies the frequency and duty cycle on the CLK contact.

Test Code
1CB.013.0x

Reference
This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions
Use Table 17 for the test conditions during verifications of the voltage perturbations on the CLK contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>ICC</th>
<th>ICLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10 μA ± 1 μA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10 μA ± 1 μA</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-49 μA ± 1 μA</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-49 μA ± 1 μA</td>
</tr>
</tbody>
</table>

Table 17 – Test conditions for 1CB.013.0x

Procedure
Follow this procedure to verify the voltage trends on the CLK contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 17.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK frequency and duty cycle between contacts C3 (CLK) and C5 (GND) when RST is at high state. Retain the minimum, maximum and average frequencies.

If the measurement system is limited to observations shorter than the whole transaction, the measurements shall be done at least 10 times, during at least 50 ms each and at intervals of at least 50 ms, when RST is at high state during the transaction. For each interval, the average CLK frequency for this interval (f_i) shall be computed. At the end of the test, the CLK average frequency shall be computed as the mathematical average of the results for all intervals:

\[ \text{CLK average frequency} = \frac{1}{n} \times \Sigma_{i=1}^{n} f_i \]
6. Set the test conditions as listed in the next line of Table 17 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met at any time when RST is at high state during the whole monitoring duration and under all environmental and test conditions:

1. \((1 \text{ MHz} - \varepsilon\text{Hz}) \leq \text{CLK frequency} \leq (5 \text{ MHz} + \varepsilon\text{Hz})\)
2. \([\max(f) \cdot \varepsilon\text{Hz}] \leq (101\% \text{ of CLK average frequency})\)
3. \([\min(f) + \varepsilon\text{Hz}] \geq (99\% \text{ of CLK average frequency})\)
4. \((45\% - \varepsilon\%) \leq \text{CLK duty cycle} \leq (55\% + \varepsilon\%)\)

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.15 1CB.014.0x - RST voltage

This test verifies the voltage trends on the RST contact.

Test Code
1CB.014.0x

Reference
This test refers to requirements in [D01], section 5.5.5, Table 13.

Test Conditions
Use Table 18 for the test conditions during verifications of the voltage trends on the RST contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>I_{CC}</th>
<th>I_{RST}</th>
<th>Trigger delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA -49 μA ± 1 μA</td>
<td>320 ns</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA -49 μA ± 1 μA</td>
<td>320 ns</td>
</tr>
</tbody>
</table>

Table 18 – Test conditions for 1CB.014.0x

Procedure
Follow this procedure to verify the voltage trends on the RST contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 18.
3. Initiate cold reset.
4. Wait for V_{CC} to be activated.
5. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
6. Wait for V_{CC} to be deactivated.
7. During steps 4 to 6, monitor the RST voltage between contacts C2 (RST) and C5 (GND).
8. Set the test conditions as listed in the next line of Table 18 and repeat steps 3 to 7.
9. Repeat steps 1 to 8 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. (-50 mV + εV) ≤ Low state RST voltage ≤ ((0.15 × V_{CC}) + εVV)
2. ((0.8 × V_{CC}) + εVV) ≤ High state RST voltage ≤ (V_{CC} + 50 mV + εVV)

To be recognized as a failed test, a non-compliance situation shall last at least for the trigger delay duration.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.16 1CB.015.0x - RST rise and fall times

This test verifies the rise and fall times on the RST contact.

Test Code
1CB.015.0x

Reference
This test refers to requirements in [D01], section 5.5.5, Table 13.

Test Conditions
Use Table 19 for the test conditions during verifications of the rise and fall times on the RST contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Icc</th>
<th>Irst</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA ± 10 μA ± 1 μA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA ± 10 μA ± 1 μA</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA ± 49 μA ± 1 μA</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA ± 49 μA ± 1 μA</td>
</tr>
</tbody>
</table>

Table 19 – Test conditions for 1CB.015.0x

Procedure
Follow this procedure to verify the rise and fall times on the RST contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 19.
3. Initiate cold reset.
4. Wait for \( V_{cc} \) to be activated.
5. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
6. Wait for \( V_{cc} \) to be deactivated.
7. During steps 4 to 6, monitor the RST rise time (10% to 90% of \( 0.2 \times V_{cc} \) to \( 0.7 \times V_{cc} \)) and the RST fall time (90% to 10% of \( 0.7 \times V_{cc} \) to \( 0.2 \times V_{cc} \)) between contacts C2 (RST) and C5 (GND).
8. Set the test conditions as listed in the next line of Table 19 and repeat steps 3 to 7. Repeat this step until the end of the table.
9. Repeat steps 1 to 8 for all other environmental conditions.
Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:
1. RST rise time \( \leq (800 \text{ ns} + \epsilon s) \)
2. RST fall time \( \leq (800 \text{ ns} + \epsilon s) \)

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.17 1CB.016.0x - RST signal perturbations

This test verifies the voltage perturbations on the RST contact.

**Test Code**
1CB.016.0x

**Reference**
This test refers to requirements in [D01], section 5.5.5, Table 13.

**Test Conditions**
Use Table 20 for the test conditions during verifications of the voltage perturbations on the RST contact.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>ICC</th>
<th>I_{RST}</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10 μA ± 1 μA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+10 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-10 μA ± 1 μA</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-49 μA ± 1 μA</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>+49 μA ± 1 μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-49 μA ± 1 μA</td>
</tr>
</tbody>
</table>

Table 20 – Test conditions for 1CB.016.0x

**Procedure**
Follow this procedure to verify the voltage perturbations on the RST contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 20.
3. Initiate cold reset.
4. Wait for V_{CC} to be activated.
5. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
6. Wait for V_{cc} to be deactivated.
7. During steps 4 to 6, monitor the RST voltage between contacts C2 (RST) and C5 (GND).
8. Set the test conditions as listed in the next line of Table 20 and repeat steps 3 to 7. Repeat this step until the end of the table.
9. Repeat steps 1 to 8 for all other environmental conditions.
Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. 
   
   \((-0.25 \text{ V} \cdot \varepsilon \text{V}) \leq \text{RST voltage} \leq (V_{CC} + 0.25 \text{ V} + \varepsilon \text{VV})\)

2. 
   
   Each time that the RST voltage increases over \(((0.2 \times V_{CC}) + \varepsilon \text{VV}), it reaches next
   
   \(((0.7 \times V_{CC}) \cdot \varepsilon \text{VV})\) or above before decreasing again under \(((0.2 \times V_{CC}) + \varepsilon \text{VV}).\)

3. 
   
   Each time that the RST voltage decreases under \(((0.7 \times V_{CC}) \cdot \varepsilon \text{VV}), it reaches
   
   next \(((0.2 \times V_{CC}) + \varepsilon \text{VV})\) or below before increasing again over \(((0.7 \times V_{CC}) \cdot \varepsilon \text{VV}).\)

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.18 1CB.017.xx - $V_{CC}$ voltage

This test verifies the voltage on the VCC contact.

**Test Code**

1CB.017.0x

**Reference**

This test refers to requirements in [D01], section 5.5.6, Table 14.

**Test Conditions**

Use Table 21 for the test conditions during verifications of the voltage on the VCC contact.

<table>
<thead>
<tr>
<th>Value of xx</th>
<th>DUT input power supply</th>
<th>$I_{CC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Nominal (as per ICS)</td>
<td>$\leq 0.2$ mA</td>
</tr>
<tr>
<td>02</td>
<td>Nominal (as per ICS)</td>
<td>$1$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>03</td>
<td>Nominal (as per ICS)</td>
<td>$25$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>04</td>
<td>Nominal (as per ICS)</td>
<td>$54$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>05</td>
<td>Minimum (as per ICS)</td>
<td>$\leq 0.2$ mA</td>
</tr>
<tr>
<td>06</td>
<td>Minimum (as per ICS)</td>
<td>$1$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>07</td>
<td>Minimum (as per ICS)</td>
<td>$25$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>08</td>
<td>Minimum (as per ICS)</td>
<td>$54$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>09</td>
<td>Maximum (as per ICS)</td>
<td>$\leq 0.2$ mA</td>
</tr>
<tr>
<td>10</td>
<td>Maximum (as per ICS)</td>
<td>$1$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>11</td>
<td>Maximum (as per ICS)</td>
<td>$25$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
<tr>
<td>12</td>
<td>Maximum (as per ICS)</td>
<td>$54$ mA $\pm$ 2% $\pm 0.1$ mA</td>
</tr>
</tbody>
</table>

Table 21 – Test conditions for 1CB.017.0x

**Procedure**

Follow this procedure to verify the voltage on the VCC contact:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 21.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 21 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. For Class A:
   a. \((-0.25 \text{ V} - \varepsilon \text{V}) \leq \text{Vcc voltage} \leq (5.40 \text{ V} + \varepsilon \text{V})\)
   b. When CLK is active \((4.60 \text{ V} - \varepsilon \text{V}) \leq \text{Vcc voltage}\)

2. For Class B:
   a. \((-0.25 \text{ V} - \varepsilon \text{V}) \leq \text{Vcc voltage} \leq (3.24 \text{ V} + \varepsilon \text{V})\)
   b. When CLK is active \((2.76 \text{ V} - \varepsilon \text{V}) \leq \text{Vcc voltage}\)

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
6.19 1CB.018.xx - Transients neutralization on VCC

This test verifies the voltage on the VCC contact under dynamic load conditions.

Test Code
1CB.018.0x

Reference
This test refers to requirements in [D01], section 5.5.6, Table 14.

Test Conditions
Use Table 22 for the test conditions during verifications of the voltage on the VCC contact of a Class A DUT under dynamic load. All currents shall be generated with a maximum ($\pm 2\% \pm 0.1 \text{ mA}$) uncertainty.

<table>
<thead>
<tr>
<th>Value of xx</th>
<th>DUT input power supply (as per ICS)</th>
<th>Rest I$_{CC}$</th>
<th>Spike I$_{CC}$</th>
<th>Spike type</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Nominal</td>
<td>$\leq 0.2$ mA</td>
<td>95 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>02</td>
<td>Nominal</td>
<td>$\leq 0.2$ mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>03</td>
<td>Nominal</td>
<td>1 mA</td>
<td>95 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>04</td>
<td>Nominal</td>
<td>1 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>05</td>
<td>Nominal</td>
<td>25 mA</td>
<td>55 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>06</td>
<td>Nominal</td>
<td>25 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>07</td>
<td>Nominal</td>
<td>40 mA</td>
<td>25 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>08</td>
<td>Nominal</td>
<td>54 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>09</td>
<td>Minimum</td>
<td>$\leq 0.2$ mA</td>
<td>95 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>10</td>
<td>Minimum</td>
<td>$\leq 0.2$ mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>11</td>
<td>Minimum</td>
<td>1 mA</td>
<td>95 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>12</td>
<td>Minimum</td>
<td>1 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>13</td>
<td>Minimum</td>
<td>25 mA</td>
<td>55 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>14</td>
<td>Minimum</td>
<td>25 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>15</td>
<td>Minimum</td>
<td>40 mA</td>
<td>25 mA</td>
<td>Fixed</td>
</tr>
</tbody>
</table>
### Table 22 – Class A test conditions for 1CB.018.0x

Use Table 23 for the test conditions during verifications of the voltage on the VCC contact of a Class B DUT under dynamic load. All currents shall be generated with a maximum (± 2% ± 0.1 mA) uncertainty.

<table>
<thead>
<tr>
<th>Value of xx</th>
<th>DUT input power supply (as per ICS)</th>
<th>Rest I\text{CC}</th>
<th>Spike I\text{CC}</th>
<th>Spike type</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Minimum</td>
<td>54 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>17</td>
<td>Maximum</td>
<td>≤ 0.2 mA</td>
<td>95 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>18</td>
<td>Maximum</td>
<td>≤ 0.2 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>19</td>
<td>Maximum</td>
<td>1 mA</td>
<td>95 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>20</td>
<td>Maximum</td>
<td>1 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>21</td>
<td>Maximum</td>
<td>25 mA</td>
<td>55 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>22</td>
<td>Maximum</td>
<td>25 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
<tr>
<td>23</td>
<td>Maximum</td>
<td>40 mA</td>
<td>25 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>24</td>
<td>Maximum</td>
<td>54 mA</td>
<td>95 mA</td>
<td>Random</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value of xx</th>
<th>DUT input power supply (as per ICS)</th>
<th>Rest I\text{CC}</th>
<th>Spike I\text{CC}</th>
<th>Spike type</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Nominal</td>
<td>≤ 0.2 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>02</td>
<td>Nominal</td>
<td>≤ 0.2 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>03</td>
<td>Nominal</td>
<td>1 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>04</td>
<td>Nominal</td>
<td>1 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>05</td>
<td>Nominal</td>
<td>25 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>06</td>
<td>Nominal</td>
<td>25 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>07</td>
<td>Nominal</td>
<td>40 mA</td>
<td>25 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>08</td>
<td>Nominal</td>
<td>54 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>09</td>
<td>Minimum</td>
<td>≤ 0.2 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>10</td>
<td>Minimum</td>
<td>≤ 0.2 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>Value of xx</td>
<td>DUT input power supply (as per ICS)</td>
<td>Rest ICC</td>
<td>Spike ICC</td>
<td>Spike type</td>
</tr>
<tr>
<td>------------</td>
<td>------------------------------------</td>
<td>----------</td>
<td>-----------</td>
<td>------------</td>
</tr>
<tr>
<td>11</td>
<td>Minimum</td>
<td>1 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>12</td>
<td>Minimum</td>
<td>1 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>13</td>
<td>Minimum</td>
<td>25 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>14</td>
<td>Minimum</td>
<td>25 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>15</td>
<td>Minimum</td>
<td>40 mA</td>
<td>25 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>16</td>
<td>Minimum</td>
<td>54 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>17</td>
<td>Maximum</td>
<td>≤ 0.2 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>18</td>
<td>Maximum</td>
<td>≤ 0.2 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>19</td>
<td>Maximum</td>
<td>1 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>20</td>
<td>Maximum</td>
<td>1 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>21</td>
<td>Maximum</td>
<td>25 mA</td>
<td>45 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>22</td>
<td>Maximum</td>
<td>25 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
<tr>
<td>23</td>
<td>Maximum</td>
<td>40 mA</td>
<td>25 mA</td>
<td>Fixed</td>
</tr>
<tr>
<td>24</td>
<td>Maximum</td>
<td>54 mA</td>
<td>45 mA</td>
<td>Random</td>
</tr>
</tbody>
</table>

**Table 23 – Class B test conditions for 1CB.018.0x**

In Table 22 and Table 23, the “Spike type” specifies the characteristics that the ICC current shall have:

- “Fixed” spike type means that the ICC current shall present a near-square waveform, having a frequency of 5 MHz ± 0.1 MHz, a duty cycle of 50% ± 10% and a slew rate of 1.0 mA/ns ± 20%.

- “Random” spike type means that the ICC current shall present pulses with a fixed duration of 300 ns ± 30 ns for Class A and 350 ns ± 35 ns for Class B, measured at the half of the spike amplitude, then a random pause lasting between 0.1 ms and 500 ms ± 1%, and a slew rate of 1.0 mA/ns ± 20%.
In accordance with ISO 7816-3 and EMVCo Book 1 [D01], the “Spike ICC” value is the additional current flowing in the VCC contact during the spike time (i.e. on top of the rest current), while the “Rest ICC” value is the current flowing in the VCC contact in the absence of a current spike.

**Figure 6 – Definition of ICC spikes**

**Procedure**

Follow this procedure to verify the voltage on the VCC contact under dynamic load conditions:

1. Stabilize the DUT at the appropriate environmental conditions.
2. For a Class A DUT, set the test conditions as listed in the first line of Table 22. For a Class B DUT, set the test conditions as listed in the first line of Table 23.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 22 (for a Class A DUT) or Table 23 (for a Class B DUT) and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

**Acceptance criteria**

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions:

1. For Class A:
   a. \((-0.25 \text{ V} + \varepsilon\text{V}) \leq \text{Vcc voltage} \leq (5.40 \text{ V} + \varepsilon\text{V})\)
   b. When CLK is active: \((4.60 \text{ V} + \varepsilon\text{V}) \leq \text{Vcc voltage}\)

2. For Class B:
   a. \((-0.25 \text{ V} + \varepsilon\text{V}) \leq \text{Vcc voltage} \leq (3.24 \text{ V} + \varepsilon\text{V})\)
   b. When CLK is active: \((2.76 \text{ V} + \varepsilon\text{V}) \leq \text{Vcc voltage}\)

**Expected Results**

Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
7 Card Session Test Cases

7.1 1CC.001.0x - Contacts activation sequence

This test verifies the contacts activation sequence.

Test Code
1CC.001.0x

Reference
This test refers to requirements in [D01], section 6.1.2.

Test Conditions
Use Table 24 for the test conditions during verifications of the contacts activation sequence.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Icc</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
</tr>
</tbody>
</table>

Table 24 – Test conditions for 1CC.001.0x

Procedure
Follow this procedure to verify the contacts activation sequence:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 24.
3. Insert the measurement probe into the DUT (notional time t0, see Figure 7).
4. Record the notional time t1 when Vcc rises for the first time above 0.4 V DC.
5. Record the notional time t2 when Vcc rises for the first time above (4.60 V · εV) [For Class A] or (2.76 V · εV) [For Class B].
6. Record the notional time t3 when I/O rises for the first time above ((0.2 × Vcc) + εV).
7. Record the notional time t4 when CLK rises for the first time above ((0.2 × Vcc) + εV).
8. Record the notional time t5 that is 200 clock cycles after t4.
9. Record the notional time t6 when RST rises for the first time above ((0.2 × Vcc) + εV).
10. During steps 3 to 9, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND), the I/O voltage between contacts C7 (I/O) and C5 (GND), the CLK voltage between contacts C3 (CLK) and C5 (GND) and the RST voltage between contacts C2 (RST) and C5 (GND).
11. Set the test conditions as listed in the next line of Table 24 and repeat steps 3 to 10.
12. Repeat steps 1 to 10 for all other environmental conditions.
Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions:

1. The notional events appear in the correct time sequence:
   a. For VCC: \( t_0 < t_1 < t_2 \)
   b. For I/O: \( t_2 \leq t_3 < t_5 \)
   c. For CLK: \( t_2 < t_4 \)
   d. For RST: \( t_5 < t_6 \)

2. In the time interval from \( t_0 \) to \( t_2 \):
   a. \((-0.25 \text{ V DC} + \epsilon \text{ V}) \leq \text{I/O voltage} \leq (V_{CC} + 0.25 \text{ V} + \epsilon \text{ V})\)
   b. \((-0.25 \text{ V DC} + \epsilon \text{ V}) \leq \text{CLK voltage} \leq (V_{CC} + 0.25 \text{ V} + \epsilon \text{ V})\)
   c. \((-0.25 \text{ V DC} + \epsilon \text{ V}) \leq \text{RST voltage} \leq (V_{CC} + 0.25 \text{ V} + \epsilon \text{ V})\)
   d. \((-0.25 \text{ V DC} + \epsilon \text{ V}) \leq V_{CC} \text{ voltage}\)

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
7.2 1CC.002.0x - Contacts deactivation sequence

This test verifies the contacts deactivation sequence.

**Test Code**

1CC.002.0x

**Reference**

This test refers to requirements in [D01], section 6.1.5.

**Test Conditions**

Use Table 25 for the test conditions during verifications of the contacts deactivation sequence.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>I_CC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
</tr>
</tbody>
</table>

Table 25 – Test conditions for 1CC.002.0x

**Procedure**

Follow this procedure to verify the contacts activation sequence:

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 25.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. Record the notional time t₁ when RST falls for the first time below ((0.2 × V_CC) - εV) at the end of the transaction (See Figure 8).
6. Record the notional time t₂ when I/O falls for the last time below ((0.2 × V_CC) - εV) at the end of the transaction.
7. Record the notional time t₃ when CLK falls for the last time below ((0.2 × V_CC) - εV) at the end of the transaction.
8. Record the notional time t₄ when V_CC falls below (4.60 V - εV) [For Class A] or (2.76 V - εV) [For Class B].
9. Record the notional time t₅ when V_CC falls for the first time below (0.40 V - εV).
10. Record the notional time t₆ that is 100 ms after t₁.
11. During steps 5 to 10, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND), the I/O voltage between contacts C7 (I/O) and C5 (GND), the CLK voltage between contacts C3 (CLK) and C5 (GND) and the RST voltage between contacts C2 (RST) and C5 (GND).
12. Set the test conditions as listed in the next line of Table 25 and repeat steps 3 to 11.
13. Repeat steps 1 to 12 for all other environmental conditions.
Figure 8 – Contacts Deactivation Sequence

Note: In the Figure 8, the relative position of $t_2$ and $t_3$ is indicative only, for the sake of the drawing clarity. It is allowed that $t_2 < t_3$, or $t_2 = t_3$, or $t_2 > t_3$.

Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions:

1. The notional events appear in the correct time sequence:
   a. For VCC: $t_1 < t_4 < t_5 < t_6$
   b. For I/O: $t_1 < t_2 < t_4$
   c. For CLK: $t_1 < t_3 < t_4$

2. In the time interval from $t_4$ to $t_5$:
   a. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq V_{cc} \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$
   b. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq I/O \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$
   c. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq \text{CLK} \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$
   d. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq \text{RST} \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$

3. In the time interval from $t_5$ to $t_6$:
   a. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq V_{cc} \leq (0.40 \text{ V} + 0.25 \text{ V} + \varepsilon \text{V})$
   b. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq I/O \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$
   c. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq \text{CLK} \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$
   d. $(-0.25 \text{ V DC} \cdot \varepsilon \text{V}) \leq \text{RST} \leq (V_{cc} + 0.25 \text{ V} + \varepsilon \text{VV})$

Expected Results

Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
7.3 1CC.003.0x - Cold reset

This test verifies the cold reset sequence.

Test Code
1CC.003.0x

Reference
This test refers to requirements in [D01], section 6.1.3.1.

Test Conditions
Use Table 26 for the test conditions during verifications of the cold reset sequence.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Icc</th>
<th>ATR delay</th>
<th>Delay uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>400 clock cycles</td>
<td>±0 ±20 clock cycles</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>400 clock cycles</td>
<td>±0 ±20 clock cycles</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>40'000 clock cycles</td>
<td>±20 ± 0 clock cycles</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>40'000 clock cycles</td>
<td>±20 ±0 clock cycles</td>
</tr>
</tbody>
</table>

Table 26 – Test conditions for 1CC.003.0x

Procedure
Follow this procedure to verify the cold reset sequence:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 26.
3. Insert the measurement probe into the DUT. Initiate activation.
4. Record the notional time \( t_1 \) when CLK rises for the first time above \((0.7 \times Vcc) - \varepsilon V\).
5. Record the notional time \( t_2 \) when RST rises for the first time above \((0.7 \times Vcc) - \varepsilon V\).
6. Starting from \( t_2 \), wait for the delay specified in the “ATR delay” column of the concerned line of Table 26, then send the default \( T=0 \) ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of one second.
7. Set the test conditions as listed in the next line of Table 26 and repeat steps 3 to 6. Repeat this step until the end of the table.
8. Repeat steps 1 to 7 for all other environmental conditions.

Acceptance criteria
The following acceptance criteria shall be met under all environmental and test conditions:
1. The time between \( t_1 \) and \( t_2 \) is between 40'000 and 45'000 clock cycles.
2. Each sequence of commands and answers is performed correctly.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.
7.4 1CC.004.0x - Warm reset

This test verifies the warm reset sequence.

**Test Code**
1CC.003.0x

**Reference**
This test refers to requirements in [D01], section 6.1.3.2.

**Test Conditions**
Use Table 27 for the test conditions during verifications of the warm reset sequence.

<table>
<thead>
<tr>
<th>Value of x</th>
<th>Icc</th>
<th>ATR delay</th>
<th>Delay uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>400 clock cycles</td>
<td>±0 +20 clock cycles</td>
</tr>
<tr>
<td>2</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>400 clock cycles</td>
<td>±0 +20 clock cycles</td>
</tr>
<tr>
<td>3</td>
<td>2 mA ± 2% ± 0.1 mA</td>
<td>40'000 clock cycles</td>
<td>±20 ± 0 clock cycles</td>
</tr>
<tr>
<td>4</td>
<td>54 mA ± 2% ± 0.1 mA</td>
<td>40'000 clock cycles</td>
<td>±20 +0 clock cycles</td>
</tr>
</tbody>
</table>

**Table 27 – Test conditions for 1CC.004.0x**

**Procedure**
Follow this procedure to verify the warm reset sequence:
1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 27.
3. Initiate warm reset by sending the non-standard T=0 ATR “3B 60 05 00”.
4. Record the notional time \( t_1 \) when RST falls below \( ((0.2 \times V_{cc}) + \varepsilon V) \).
5. Record the notional time \( t_2 \) when RST rises above \( ((0.7 \times V_{cc}) - \varepsilon V) \).
6. Starting from \( t_2 \), wait for the delay specified in the “ATR delay” column of the concerned line of Table 27, then send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of one second.
7. Set the test conditions as listed in the next line of Table 27 and repeat steps 3 to 6. Repeat this step until the end of the table.
8. Repeat steps 1 to 7 for all other environmental conditions.
Acceptance criteria
The following acceptance criteria shall be met under all environmental and test conditions:

1. The time between \( t_1 \) and \( t_2 \) is between 40'000 and 45'000 clock cycles.

2. In the time interval from \( t_1 \) to \( t_2 \):
   a. For Class A: \( (4.60 \, \text{V} - \varepsilon \text{V}) \leq \text{Vcc voltage} \leq (5.40 \, \text{V} + \varepsilon \text{V}) \)
      For Class B: \( (2.76 \, \text{V} - \varepsilon \text{V}) \leq \text{Vcc voltage} \leq (3.24 \, \text{V} + \varepsilon \text{V}) \)
   b. \( ((0.7 \times V_{\text{CC}}) - \varepsilon \text{V}) \leq \text{I/O voltage} \leq (V_{\text{CC}} + 0.25 \, \text{V} + \varepsilon \text{V}) \)
   c. The clock is active with no interruption.

3. Each sequence of commands and answers is performed correctly.

Expected Results
Results are recorded with one of two statements:
- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

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